The I^2C Management Bus

The I^2C Management Bus is a two wire serial bus used for connecting microcontrollers and their peripheral devices. It was developed in the early 1980s by Philips semiconductor. Originally its purpose was to provide an easy way to connect a CPU to peripheral chips in television sets. The name, I^2C, is an acronym for inter-integrated circuit bus which literally explains its function: to provide a communication link between integrated circuits.

Today, the I^2C bus is being used for "server management." In servers and other devices, the I^2C management bus is used to communicate the status of individual components. For instance, a query can be made of various components to find out the configuration of the system. The I^2C bus can be also be asked for the functional status of components such as power supplies and system fans.

Physically the I^2C Bus consists of a bi-directional two-wire design consisting of a Serial Data Line (SNA) and a Serial Clock Line (SCL). A primary advantage of the bus is its simplicity and efficiency. The bus takes up very little space because the interface is directly on the component. This leads to reduced board space and pin count thereby lowering interconnectivity costs. The length of the bus can be up to 25 feet and may support as many as 40 components at a maximum transfer rate of 100 kilobits per second.

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Device Configuration

The I²C bus configuration is a combination of microcontrollers and peripheral controllers with each device having a unique bus address. The devices may take on different roles depending on the task they are performing at the moment. These roles include:

- Transmitter - a device which transmits signals over the bus.
- Receiver - a device which receives signals.
- Master - a device which controls signal transfer and clock frequency.
- Slave - a device which is controlled by the master.

Not all devices can perform all functions. For example, an LCD driver may only be a receiver, but a memory or I/O chip could be a receiver or a transmitter.

An integrated circuit (IC) which issues commands on the bus is considered the bus master. All other devices are considered the bus slaves. The I²C protocol supports multimastering in which any IC capable of initiating data transfer may be considered the bus master during its cycle.

How It Works

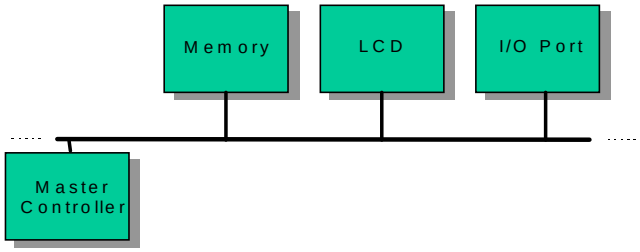
First we need to know how the devices communicate with one another. There are six codes that are used on an I²C bus:

- A start bit
- A 7 bit slave address
- A read/write bit which defines the device as a transmitter or receiver
- An acknowledge bit
- Message bits divided into 8 bit segments
- A stop bit

Consider the following scenario:

A Master Controller wants to communicate with the I/O port.

I²C Bus Example



The Master Controller issues a start bit. The start bit acts as a wake up call to all other ICs connected to the bus and causes them to listen for incoming data. The Master Controller then sends an acknowledge signal and the address of the device with which it wishes to communicate. All ICs on the bus compare the address with their own and if the addresses match, the device sends a response on the acknowledge signal back to the Master Controller. The devices that do not have matching addresses do nothing and wait for a stop bit which releases the bus. (The master always generates the start and stop conditions.)

The matching device then pulls the data line low which is an indication to the Master Controller that the device with the matching address is on the bus. The Master Controller can now begin transmitting data. At the conclusion of data transfer a stop condition is issued by the master and the bus is released.

Multiple Masters and Collision Detection

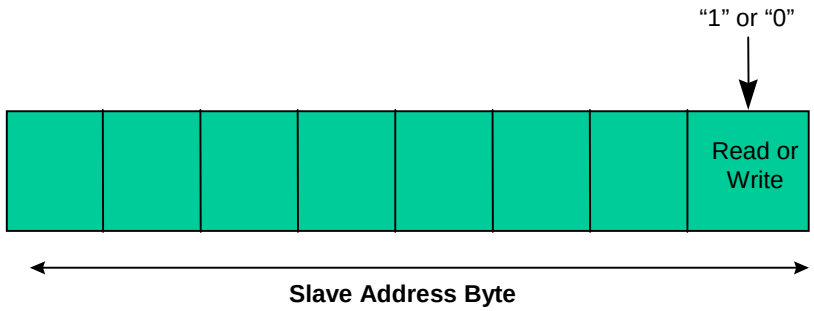
The I²C bus may contain more than one master device. The key is that there can only be one master at any point in time and that master will control the bus clock. When two (or more) devices seek to control the bus at the same time, an arbitration procedure will take place. One device will transmit a high level signal and the other competing device will transmit a lower level signal. The device transmitting the low level will take control of the bus and become the master device. The device transmitting the high level will release the bus and switch to the slave receiver mode.

Formats and Addressing

The I²C standard supports three data transfer formats. They are:

- Master transmitter writes to slave, no direction change.
- Master reads immediately after sending the address byte.
- Combined format with multiple read or write transmits.

The 7-bit address of an I²C device and the direction of the following data is coded in the first byte after the start condition. A “0” in the least significant bit indicates the master will write information to the slave device. A “1” indicates that the master will read information from the slave.



Key Points to Remember

- The I²C Management Bus is a two wire serial bus used for connecting microcontrollers and their peripheral devices.
- The I²C Management Bus is used for server management.
- I²C supports multimastering which allows any device capable of transmitting and receiving to become the bus master.
- Maximum length is 25 feet and can support up to 40 devices.
- Maximum transfer rate is 100 kilobits per second
- The I²C Bus was originally developed for audio and video equipment in the 1980s.